Amendments to the Claims

The following listing of claims replaces all prior versions and listings of claims in the application:

1. (Currently Amended) A method for VLSI design analysis, the method comprising:
in a processor, finding a loop in a circuit design;
in the processor, functionally analyzing the loop; ~~and~~
in the processor, extracting a logical element in relation to the analysis result; and
in the processor, automatically resolving the loop by performing an operation selected from a group consisting of: replacing the loop with a state element in a Finite State Machine level, and replacing the loop by a logically equivalent pure combinational non-loop logic.

2. (Original) The method of claim 1, comprising performing a Depth First Search linear traversal.

3. (Original) The method of claim 1, comprising identifying a group of at least one Channel Connected Sub-Network that forms at least one combinational loop and corresponds to a functional device.

4. (Original) The method of claim 3, comprising generating overall zero-delay collapsed functionality on an output of said group.

5. (Original) The method of claim 3, comprising identifying a functional part that forms said group.

6. (Original) The method of claim 3, comprising determining a driving logic of said group.

7. (Original) The method of claim 3, comprising determining a driving control of said group.

8. (Original) The method of claim 3, comprising determining a stage feedback logic of said group.

9. (Original) The method of claim 3, comprising determining a stage feedback control of said group.

10. (Original) The method of claim 3, comprising determining a stage feedback type of said group.

11. (Original) The method of claim 3, comprising determining an asynchronous set and reset logics of said group.

12. (Currently Amended) The method of claim 1, ~~comprising~~ wherein extracting a logical element comprises extracting a combinational logical element.

13. (Original) The method of claim 12, comprising performing an analysis of a group of at least one Channel Connected Sub-Network that forms at least one combinational loop and corresponds to a functional device.

14. (Original) The method of claim 12, comprising identifying a domino element.

15. (Original) The method of claim 12, comprising identifying a bus retainer.

16. (Original) The method of claim 12, comprising identifying a latch.

17. (Original) The method of claim 12, comprising identifying a self-reset loop.

18. (Original) The method of claim 12, comprising identifying a combinatorial element.

19. (Currently Amended) An apparatus for VLSI design analysis, the apparatus comprising:
a processor to find a loop in a circuit design, functionally analyze the loop, ~~and~~ extract a logical element in relation to the analysis result, and automatically resolve the loop by performing an operation selected from a group consisting of: replacing the loop with a state element in a Finite State Machine level, and replacing the loop by a logically equivalent pure combinational non-loop logic.

20. (Original) The apparatus of claim 19, wherein the processor is to perform a Depth First Search linear traversal.

21. (Original) The apparatus of claim 19, wherein the processor is to identify a group of at least one Channel Connected Sub-Network that forms at least one combinational loop and corresponds to a functional device.

22. (Original) The apparatus of claim 21, wherein the processor is to generate overall zero-delay collapsed functionality on an output of said group.

23. (Original) The apparatus of claim 21, wherein the processor is to identify a functional part that forms said group.

24. (Original) The apparatus of claim 21, wherein the processor is to determine a driving logic of said group.

25. (Original) The apparatus of claim 21, wherein the processor is to determine a driving control of said group.

26. (Original) The apparatus of claim 21, wherein the processor is to determine a stage feedback logic of said group.

27. (Original) The apparatus of claim 21, wherein the processor is to determine a stage feedback control of said group.

28. (Original) The apparatus of claim 21, wherein the processor is to determine a stage feedback type of said group.

29. (Original) The apparatus of claim 21, wherein the processor is to determine an asynchronous set and reset logics of said group.

30. (Currently Amended) The apparatus of claim 19, wherein the processor is to extract a combinational logical element.

31. (Original) The apparatus of claim 30, wherein the processor is to perform an analysis of a group of at least one Channel Connected Sub-Network that forms at least one combinational loop and corresponds to a functional device.

32. (Original) The apparatus of claim 30, wherein the processor is to identify a domino element.

33. (Original) The apparatus of claim 30, wherein the processor is to identify a bus retainer.

34. (Original) The apparatus of claim 30, wherein the processor is to identify a latch.

35. (Original) The apparatus of claim 30, wherein the processor is to identify a self-reset loop.

36. (Original) The apparatus of claim 30, wherein the processor is to identify a combinatorial element.

37. (Currently Amended) An apparatus for VLSI design analysis, the apparatus comprising:
a dynamic random access memory; and
a processor to find a loop in a circuit design, functionally analyze the loop, ~~and~~ extract a logical element in relation to the analysis result, and automatically resolve the loop by performing an operation selected from a group consisting of: replacing the loop with a state element in a Finite State Machine level, and replacing the loop by a logically equivalent pure combinational non-loop logic.

38. (Original) The apparatus of claim 37, wherein the processor is to identify a group of at least one Channel Connected Sub-Network that forms at least one combinational loop and corresponds to a functional device.

39. (Original) The apparatus of claim 38, wherein the processor is to identify a functional part that forms said group.

40. (Currently Amended) A machine-readable medium having stored thereon a set of instructions that, if executed by a machine, cause the machine to perform a method comprising:
finding a loop in a circuit design;
functionally analyzing the loop; ~~and~~
extracting a logical element in relation to the analysis result; and
automatically resolving the loop by performing an operation selected from a group consisting of: replacing the loop with a state element in a Finite State Machine level, and replacing the loop by a logically equivalent pure combinational non-loop logic.

41. (Original) The machine-readable medium of claim 40, wherein the instructions result in identifying a group of at least one Channel Connected Sub-Network that forms at least one combinational loop and corresponds to a functional device.

42. (Original) The machine-readable medium of claim 41, wherein the instructions result in identifying a functional part that forms said group.